

About the Institute

K.L.N. College of Engineering has been the first self-financing co-educational Engineering College started in Madurai in 1994. The College has been affiliated to Anna University and approved by All India Council for Technical Education (AICTE). The College is located in the south eastern outskirts of Madurai and is 11Km away from Madurai city. The college runs 7 undergraduate engineering programs and 7 Master Programs including M.E. Communication Systems.

Department of ECE

The Department of ECE was started in 1994. The Department has adequate infrastructure with spacious classrooms, conference halls and well developed eight laboratories having the advanced designing tools like MATLAB, Orcad P-Spice, Xilinx, IE3D, ADS, LabView and modernized equipments like spectrum analyzer, microwave power meter, GPS kit. The department initiates the U.G., P.G. & research projects in Embedded Systems through the Centre for Embedded Systems which is based on the collaboration of institution & Embedded industry. The department library has over 1500 books and magazines and journals. AICTE, New Delhi has sanctioned fund as under MODROB scheme for modernizing Microwave Lab and DSP lab of this department.

About Tech Labs

Techlabs is an ISO 9001:2008 Company headquartered in New Delhi and having branch offices at Bangalore, Hyderabad, Pune, Kolkata Dehradun and Chennai. It has offering the Engineering Software Solutions for VLSI Design, Circuit Simulation, PCB Design, Digital Signal Processing, Embedded Systems, Communications, CAD/CAM/CAE, CNC programming, Hydraulic & Pneumatic, Mechatronics, Control Systems, Power Systems, Power Electronics, High Voltage, Renewable Energy, Machine Design. It is an authorized dealer of Tanner tools & Mentor Graphics tools.

Objectives of the Workshop

Theory Session:-

- Introduction to VLSI Design Flow –
- Front-end & Back-end Design with Mentor Graphics tools and Tanner tools
- Academic syllabus for U.G. and P.G. students on VLSI Design
- Basics of FPGA & Details about Altera Products & Architecture overview

Demonstration & Hands-on Session:-

- Simulation using Modelsim
- Synthesis using Precision RTL Plus
- Configuration of Altera FPGAs
- Complete VLSI design flow using Tanner EDA tool
- Hands-on experiments are based on academic syllabus of VLSI lab

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Two-Day Workshop on “VLSI Design Flow with hands-on for Academicians”

23-08-2013 & 24-08-2013
(Friday & Saturday)

REGISTRATION FORM

Name :

Qualification :

Designation :

Experience :

Department :

Organization :

Address for :

Communication

Phone No. :

Mobile No. :

E-mail id :

Accommodation required : Yes No

Date:

Signature of the Applicant

Accommodation

No TA / DA will be paid to the participants. On prior request, accommodation can be arranged in our college hostel with breakfast & dinner at a nominal fee.

Who can Register?

The programme is open for all engineering faculty members & industrial persons. Interested Research Scholars are also allowed to register. Application can be downloaded from the website www.klnce.edu

Registration Fee includes

- 1) Course Kit (Provided by Tech Labs)
- 2) Course Materials (Provided by Tech Labs)
- 3) FDP Certificate (Provided by Tech Labs)
- 4) Working Lunch, Tea & Snacks

Registration Fee

No registration fees for this event.

Local Transportation

Our college buses are plying on daily over 15 routes from various parts of city. Participants can use these buses to reach K.L.N.C.E. For further information please contact coordinators.

Academic Correspondence:

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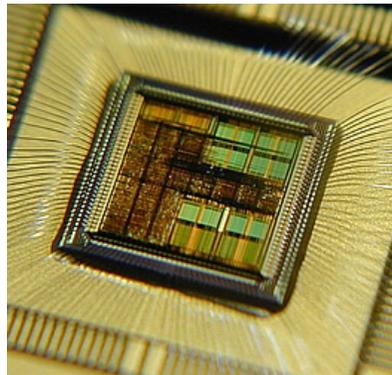
Program Schedule

Day-1:-

- 08:45 - 09:15 – Registration
09:15 - 09:30 – Inauguration
09:30 - 09:45 – Address by Techlabs
09:45 - 10:30 – Presentation on
VLSI FPGA Design Flow
10:30 - 10:45 – Tea Break
10:45 - 11:45 – Presentation on
Mentor Graphics Tools.
11:45 - 12:30 – Demonstration on
Modelsim & Precision RTL+ Synthesis
& Altera FPGA Platform
12:30 - 01:30 – Lunch Break
01:30 - 03:15 – Hands on
Modelsim & Precision RTL+ Synthesis
03:15 - 03:30 – Tea Break
03:15 - 04:40 – Hands on
Modelsim & Precision RTL+ Synthesis
& Altera FPGA Platform

Day-2:-

- 09:00 - 09:45 – Presentation on
VLSI ASIC Design Flow
09:45 - 10:30 – Presentation on Tanner EDA tools
10:30 - 10:45 – Tea Break
10:45 - 11:45 – Demonstration on Tanner EDA flow
11:45 - 12:30 – Hands on Tanner Tools (Session - I)
12:30 - 01:30 – Lunch Break
01:30 - 03:15 – Hands on Tanner Tools (Session - II)
03:15 - 03:30 – Tea Break
03:30 - 04:00 – General Review on
Mentor Graphics & Tanner EDA
04:00 - 04:30 – Feedback and Conclusion



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**Chairman
Dr.A.V.Ramprasad, Principal**

**Convener & H.O.D - ECE
Prof.V.Kejalakshmi**

**Coordinators
Mr.N.Janakiraman
Mr. V.Muthu Ganesh**



**Organized by
Department of Electronics & Communication
Engineering**

(Accredited by NBA, New Delhi)
K.L.N.COLLEGE OF ENGINEERING

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